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1 Organization and performance of a two-level virtual-real cache hierarchy
W. H. Wang, J.-L. Baer, H. M. Levy
April 1989 **ACM SIGARCH Computer Architecture News , Proceedings of the 16th annual international symposium on Computer architecture**, Volume 17 Issue 3
Full text available: pdf(1.01 MB) Additional Information: full citation, abstract, references, citings, index terms

We propose and analyze a two-level cache organization that provides high memory bandwidth. The first-level cache is accessed directly by virtual addresses. It is small, fast, and, without the burden of address translation, can easily be optimized to match the processor speed. The virtually-addressed cache is backed up by a large physically-addressed cache; this second-level cache provides a high hit ratio and greatly reduces memory traffic. We show how the second-level cache can be easily e ...

2 A memory management unit and cache controller for the MARS system
Feipei Lai, Chyuan-Yow Wu, Tai-Ming Parng
November 1990 **Proceedings of the 23rd annual workshop and symposium on Microprogramming and microarchitecture**
Full text available: pdf(1.07 MB) Additional Information: full citation, abstract, references

For large caches, the interaction between cache access and address translation affects the machine cycle time and the access time to memory. The physically addressed caches slow down the cache access due to the virtual address translation. The virtually addressed caches is faster, but the synonym problem is difficult to handle. By some software constraints and hardware support, our virtually addressed physically tagged caches can achieve the same speed as traditional virtually addressed cac ...

3 Supporting reference and dirty bits in SPUR's virtual address cache
D. A. Wood, R. H. Katz
April 1989 **ACM SIGARCH Computer Architecture News , Proceedings of the 16th annual international symposium on Computer architecture**, Volume 17 Issue 3
Full text available: pdf(1.12 MB) Additional Information: full citation, abstract, references, citings, index terms

Virtual address caches can provide faster access times than physical address caches, because translation is only required on cache misses. However, because we don't check the translation information on each cache access, maintaining reference and dirty bits is more difficult. In this paper we examine the trade-offs in supporting reference and dirty bits in a virtual address cache. We use measurements from a uniprocessor SPUR prototype to evaluate different alternatives. The prototype's buil ...

4 Coherency for multiprocessor virtual address caches

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1 **Synonym hit RAM - a 500-MHz CMOS SRAM macro with 576-bit parallel comparison and parity check functions**
Suzuki, T.; Higeta, K.; Fujimura, Y.; Ando, K.; Nambu, H.; Yamagata, R.; Hotta, A.; Yamaguchi, K.;
Solid-State Circuits, IEEE Journal of , Volume: 35 , Issue: 2 , Feb. 2000
Pages:163 - 174

[Abstract] [PDF Full-Text (280 KB)] **IEEE JNL**

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2 **Information technology - portable operating system interface (POSIX) part 4: rationale**

ISO/IEC 9945-4. Rationale, IEEE Std 1003.1, 2003 Edition , 2003
Pages:0_1 - 310

[Abstract] [PDF Full-Text (1869 KB)] **IEEE STD**

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3 **1003.1 standard for information technology portable operating system interface (posix) rationale (informative)**

IEEE Std 1003.1-2001. Rationale (Informative) , 2001
Pages:i - 310

[Abstract] [PDF Full-Text (1664 KB)] **IEEE STD**

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4 **Virtual page tag reduction for low-power TLBs**
Petrov, P.; Orailoglu, A.;
Computer Design, 2003. Proceedings. 21st International Conference on , 13-15 Oct. 2003
Pages:371 - 374